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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,077	03/14/2001	Takuya Ishida	108108	1463
25944	7590	11/05/2004	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			CASIANO, ANGEL L	
			ART UNIT	PAPER NUMBER
			2182	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/787,077	Applicant(s) ISHIDA ET AL.	
	Examiner Angel L Casiano	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 June 2004.
 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 1-25 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment

The present Office action is in response to Amendment dated 14 June 2004.

Claims 1-25 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawande et al. [US 6,219,697 B1] in view of Fujimori et al. [US 6,108,718], in further view of Cook et al. [US 5,724,517 A].

Regarding claim 1, Lawande et al. teaches a data transfer control device (see Abstract; col. 4, line 7) for transferring data between nodes connected to a bus (see Abstract; col. 1, lines 1-4; col. 23, line 33). The cited prior art teaches identification information (see Abstract; col. 2, lines 34-42; see Fig. 6A; col. 4, line 21). A reset interval is defined by the cited prior art that clears node topology (see col. 12, lines 47-49; Figure 6A, "162"). The cited disclosure links each received packet with the generated identification information (see Abstract). Lawande et al. teaches writing the linked packet and identification information into a packet storage (see col. 23, lines

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35-44). However, Lawande et al. does not explicitly teach a *circuit* which *generates identification information* for determining whether or not one received packet and the next received packet are received during different reset intervals, as claimed. Fujimori et al. teaches a method for information delivery including a circuit, which generates identification information and determines if a packet has been received during a reset interval (see col. 8, lines 6-24). Accordingly, one of ordinary skill in the art would have been motivated to combine the cited references in order to reduce the number of communication of control signals and apply this improvement to systems using an IEEE 1394 serial bus (see Fujimori et al., col. 1, lines 5-11). The combination of references does not explicitly cite a *pointer* that specifies a boundary in memory between packets received before and after the reset. Regarding this limitation, Cook et al. explicitly teaches a pointer (see Figure 3) that indicates packets before and after the occurrence of the reset (see Abstract; col. 7, lines 38-64). Cook et al. explicitly cites that in order to construct a bus topology map; the ID packets must have been stored in memory (see col. 6, lines 16-18). At the time of the invention, one of ordinary skill in the art would have been motivated to modify the combination of references in order to obtain a method for obtaining topology information which optimizes delay and speed between nodes, as taught by Cook et al (col. 1, lines 43-44).

As for claim 2, the combination of references teaches identification information for determining whether a packet was received before or after a reset (see Cook et al.; Figure 3). As part of this information, Cook et al. initializes a "Root Node ID" to 0. This value changes based upon on a comparison (see Figure 3, "314-318").

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Regarding claim 3, Lawande et al. teaches storing packets (see col. 23, lines 35-36, 41) including control information area (inherent, see col. 23, lines 29-32) and data area (see col. 23, lines 51-54). The cited art also discloses identification information as part of the control information (see “identifier”, col. 23, lines 29-32). The cited reference does not specify the storage means (see “memory”) as randomly accessible. However, randomly accessible memory is well known in the art, since it retains its contents when power is turned off. Therefore, one of ordinary skill in the art would have been motivated to specify the cited storage means as randomly accessible, in order to obtain a memory which has the information permanently placed into it.

Regarding claim 10, Lawande et al. teaches a data transfer control device for transferring data between a plurality of nodes connected to a bus (see Abstract). The cited disclosure includes read means for reading a packet from storage when a transmission start command has been issued (see col. 12, lines 56-58) as well as link means for transmitting read packet to each node (see col. 12, lines 61-63). Lawande et al. also teaches status storage, indicating that transmission has been halted (see “stopped”, col. 13, line 57) by the occurrence of a reset (see col. 12, lines 41-43, 46-50). The combination of reference does not explicitly cite a pointer that specifies a boundary in memory between packets received before and after the reset. Regarding this limitation, Cook et al. explicitly teaches a pointer (see Figure 3) that indicates packets before and after the occurrence of the reset (see Abstract; col. 7, lines 38-64). Cook et al. explicitly cites that in order to construct a bus topology map; the ID packets must have been stored in memory (see col. 6, lines 16-18). At the time of the invention, one of ordinary skill in the art would have been motivated to modify the combination of references for the reasons stated in claim 1.

As for claim 11, the cited art (Lawande) exposes processing means for issuing the transmission start command (see col. 12, line 58; Fig. 6A). The processing means included in the reference cancels transmission processing that has already started (see col. 12, lines 56-57) without determining whether or not transmission has been completed when it has been determined from the status information that transmission of a packet has been halted by the occurrence of the reset (see “reset”, col. 12, line 39; Fig. 6A).

As for claim 12, the data transfer control device disclosed by Lawande et al. teaches a bus reset as defined by the IEEE 1394 standard (see Abstract; col. 12, lines 50-53; col. 25, lines 11-15).

As for claim 14, the data transfer control device disclosed by Lawande et al. teaches a bus reset as defined by the IEEE 1394 standard (see Abstract; col. 12, lines 50-53; col. 25, lines 11-15).

As for claim, 15, the data transfer control device disclosed by Lawande et al. includes data transfer according to the IEEE 1394 standard (see Abstract; col. 25, lines 20-21).

As for claim 17, the data transfer control device disclosed by Lawande et al. includes data transfer according to the IEEE 1394 standard (see Abstract; col. 25, lines 20-21).

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As for independent claims 18 and 21, these constitute the electronic equipment including the data transfer control device as disclosed in claim 1. Claim 1 is rejected in the present Office action. Therefore, claims 18 and 21 are rejected under the same rationale.

As for independent claims 20 and 23, these constitute the electronic equipment including the data transfer control device as disclosed in claim 10. Claim 10 is rejected in the present Office action. Accordingly, claims 20 and 23 are rejected under the same rationale.

Regarding claim 24, Lawande et al. teaches a data transfer control device (see Abstract; col. 4, line 7) for transferring data between nodes connected to a bus (see Abstract; col. 1, lines 1-4; col. 23, line 33). The cited prior art teaches identification information (see Abstract; col. 2, lines 34-42; see Fig. 6A; col. 4, line 21). A reset interval is defined by the cited prior art that clears node topology (see col. 12, lines 47-49; Figure 6A, "162"). The cited disclosure links each received packet with the generated identification information (see Abstract). Lawande et al. teaches writing the linked packet and identification information into a packet storage (see col. 23, lines 35-44). However, Lawande et al. does not explicitly teach a *circuit* which generates identification information for determining whether or not one received packet and the next received packet are received during different reset intervals, as claimed. Fujimori et al. teaches a method for information delivery including a circuit, which generates identification information and determines if a packet has been received during a reset interval (see col. 8, lines 6-24). Accordingly, one of ordinary skill in the art would have been motivated to combine the cited references in order to reduce the number of communication of control signals and apply this

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improvement to systems using an IEEE 1394 serial bus (see Fujimori et al., col. 1, lines 5-11). The combination of references does not explicitly cite a “changing point” that specifies a boundary in memory between packets received before and after the reset. Regarding this limitation, Cook et al. explicitly teaches a pointer (see Figure 3) that indicates packets before and after the occurrence of the reset (see Abstract; col. 7, lines 38-64). Cook et al. explicitly cites that in order to construct a bus topology map; the ID packets must have been stored in memory (see col. 6, lines 16-18). At the time of the invention, one of ordinary skill in the art would have been motivated to modify the combination of references in order to obtain a method for obtaining topology information which optimizes delay and speed between nodes, as taught by Cook et al (col. 1, lines 43-44).

As for claim 25, Lawande et al. teaches storing packets (see col. 23, lines 35-36, 41) including control information area (inherent, see col. 23, lines 29-32) and data area (see col. 23, lines 51-54). The cited art also discloses identification information as part of the control information (see “identifier”, col. 23, lines 29-32). The cited reference does not specify the storage means (see “memory”) as randomly accessible. However, randomly accessible memory is well known in the art, since it retains its contents when power is turned off. Therefore, one of ordinary skill in the art would have been motivated to specify the cited storage means as randomly accessible, in order to obtain a memory which has the information permanently placed into it.

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3. Claims 4-9, 13, 16, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawande et al. [US 6,219,697 B1] in view of Fujimori et al. [6,108,718] in further view of Gehman et al. [US 6,304,553 B1].

Regarding claims 4 and 5, the combination of references teaches a data transfer control device (see Abstract; col. 4, line 7) for transferring data between nodes connected to a bus (see Abstract; col. 1, lines 1-4; col. 23, line 33). However, the cited combination does not teach a first pointer storage means for storing pointer information that specifies a boundary in the packet storage means. Nonetheless, the references do teach identification for the packets received before the occurrence of a reset that clears node topology information and for packets received after the occurrence of the reset (Lawande et al., see col. 2, lines 34-38). In addition, Gehman et al. teaches a data transfer control device where pointer information specifies a boundary in storage (see col. 5, lines 48-49). One of ordinary skill in the art would have been motivated to modify the combination of references in order to obtain a data transfer control device applicable to the IEEE 1394 standard having a pointer as a reference (e.g. "start address") for a boundary.

As for claims 6 and 7, the combination of prior art teaches information for processed and unprocessed packets (see Abstract) as well as for received and not received packets. However, the prior art does not teach a second or third pointer storage means for storing pointer information that specifies a boundary in the packet storage means. Nonetheless, Gehman et al. teaches a data transfer control device where pointer information specifies a boundary in storage (see col. 5, lines 48-49). One of ordinary skill in the art would have been motivated to modify

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the cited references in order to obtain a data transfer control device applicable to the IEEE 1394 standard having a pointer as a reference for a boundary.

As for claim 8, the combination of references teaches storing packets (see col. 23, lines 35-36, 41) including control information area (inherent, see col. 23, lines 29-32) and data area (see col. 23, lines 51-54). The cited combination of prior art also discloses identification information as part of the control information (see “identifier”, col. 23, lines 29-32). However, the cited art does not teach a first pointer storage means for storing pointer information that specifies a boundary in the packet storage means, and which includes fourth and fifth pointer storage means. Nonetheless, the references do teach identification for the packets received before the occurrence of a reset that clears node topology information and for packets received after the occurrence of the reset (inherent, see col. 2, lines 34-38). Gehman et al. teaches a data transfer control device where pointer information specifies a boundary in storage (see col. 5, lines 48-49). One of ordinary skill in the art would have been motivated to modify the cited combination of references in order to obtain a data transfer control device applicable to the IEEE 1394 standard having a pointer as a reference (e.g. for “control information”) for a boundary.

As for claim 9, the combination of references teaches storing packets (see col. 23, lines 35-36, 41) including a data area (see col. 23, lines 51-54). The cited art combination also discloses identification information as part of the control information (see “identifier”, col. 23, lines 29-32). However, it does not teach a fifth pointer storage means for storing pointer information that specifies a boundary in the first data area. The prior art teaches identification for the packets

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received before the occurrence of a reset that clears node topology information and for packets received after the occurrence of the reset (inherent, see col. 2, lines 34-38). Accordingly, Gehman et al. teaches a data transfer control device where pointer information specifies a boundary in storage (see col. 5, lines 48-49). One of ordinary skill in the art would have been motivated to modify the cited combination of references in order to obtain a data transfer control device applicable to the IEEE 1394 standard having a pointer as a reference for indicating a boundary.

As for claims 13 and 16, the cited references teach a bus reset and data transfer in accordance with the IEEE 1394 standard (see Lawande et al, "Abstract"; Gehman et al., col. 5, lines 25 and 39-50). One of ordinary skill in the art would have been motivated to modify the cited combination of references in order to obtain a data transfer control device, applicable to the IEEE 1394 standard, and able to provide a reference (see "boundary") for the data processing by using a pointer.

As for independent claims 19 and 22, these are oriented to the electronic equipment including the data transfer control device, as disclosed in a previous claim (see claim 4). The previous claim is rejected in the present Office action under 35 U.S.C. 103(a). Accordingly, the present claims are being rejected under the same rationale.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3, 10-12, 14-15, 17-18, 20-21, and 23-25 have been considered but are moot in view of the new ground(s) of rejection.

5. Regarding Applicant's arguments for claims 18-23, Examiner respectfully submits that this is presumably petitionable matter.

6. As for applicant's arguments regarding claims 4-9, 13, 16, 19, and 22, Examiner respectfully disagrees. In consideration of claim 4, Lawande et al. explicitly teaches a reset interval that clears node topology (see col. 12, lines 47-49; Figure 6A, "162"). In addition, the reference teaches a memory function that examines the "protocol_type" field to determine where the packet is from and how to process it (see col. 17, lines 14-44). Lawande et al. clearly makes a distinction as to the packet's origin (see also col. 18, lines 8-40). Lawande et al. however does not teach a pointer. Gehman et al. teaches a pointer in storage, which also specifies a boundary. The combination of references would provide a system capable of determining whether a packet was received before or after a reset even and a pointer indicating this in memory. One of ordinary skill in the art would have been motivated to combine these disclosures in order to obtain an improved data processing system, as disclosed by Gehman (col. 1).

The test for obviousness under 35 U.S.C. 103 is not the express suggestion of the claimed invention in any or all of the references, but what the references taken collectively would suggest. In re Conrad, 169 USPQ 170 (CCPA 1971).

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Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Otsuka [JP2000078156A] teaches an event where power is turned off (reset) and all nodes connected to serial bus transmit self-ID packets and execute self-ID processes.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:00 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571-272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
29 October 2004.



KIM HUYNH
PRIMARY EXAMINER

10/29/04